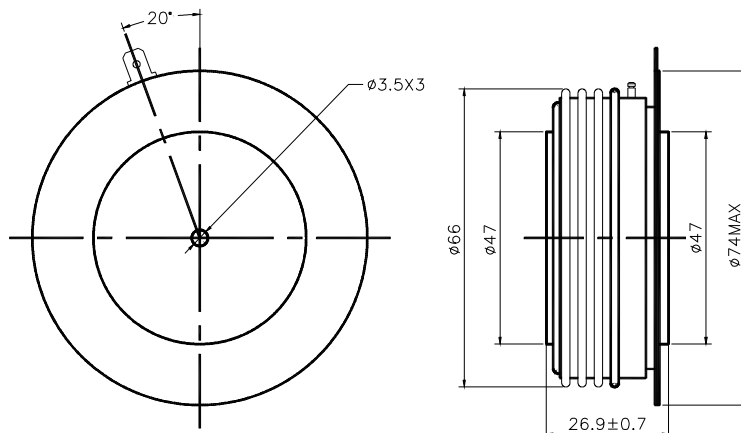


T10-XX00
PHASE CONTROL
THYRISTOR

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _j (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Double side cooled, T _{hs} =55°C	125			1270	A
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Double side cooled, T _{hs} =80°C	125			942	A
V _{DRM} V _{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V _{DRM} &V _{RRM} tp=10ms V _{DSM} &V _{RSM} = V _{DRM} &V _{RRM} +100V respectively	125	1900		2600	V
I _{DRM} I _{RRM}	Repetitive peak current	at V _{DRM} at V _{RRM}	125			80	mA
I _{TSM}	Surge on-state current	10ms half sine wave	125			17.6	KA
I ² T	I ² T for fusing coordination	V _R =0.6V _{RRM}				1548	A ² s*10 ³
V _{TO}	Threshold voltage		125			1.11	V
r _T	On-state slop resistance					0.38	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =2300A, F=24KN	125			1.99	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =0.67V _{DRM}	125			500	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V _{DRM} to 1500A, Gate source 1.5A t _r ≤0.5μs Repetitive	125			300	A/μs
I _{rm}	Reverse recovery current					180	A
t _{rr}	Reverse recovery time	I _{TM} =1000A, tp=1000μs, di/dt=-20A/μs, V _i =50V	125			18	μs
Q _{rr}	Recovery charge					1620	μC
I _{GT}	Gate trigger current			40		300	mA
V _{GT}	Gate trigger voltage	V _A =12V, I _A =1A	25	0.8		3.0	V
I _H	Holding current			20		250	mA
V _{GD}	Non-trigger gate voltage	At 67%V _{DRM}	125			0.3	V
R _{th(j-h)}	Thermal resistance Junction to heatsink	At 180° sine' double side cooled Clamping force 24KN				0.024	°C /W
F _m	Mounting force			19		26	KN
T _{stg}	Stored temperature			-40		140	°C
W _t	Weight					470	g
Outline	KT50cT						

Outline



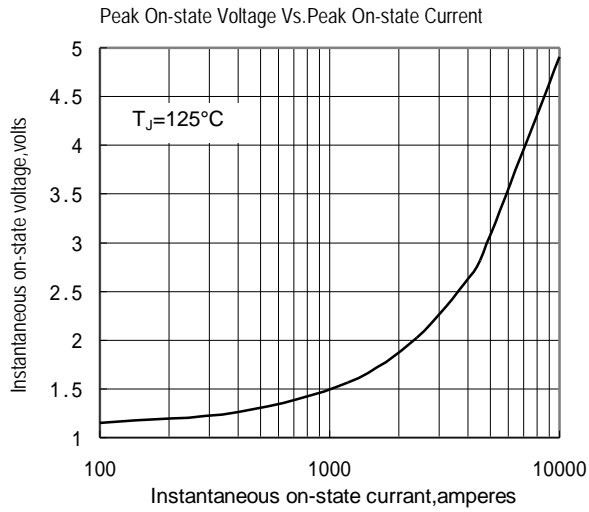


Fig.1

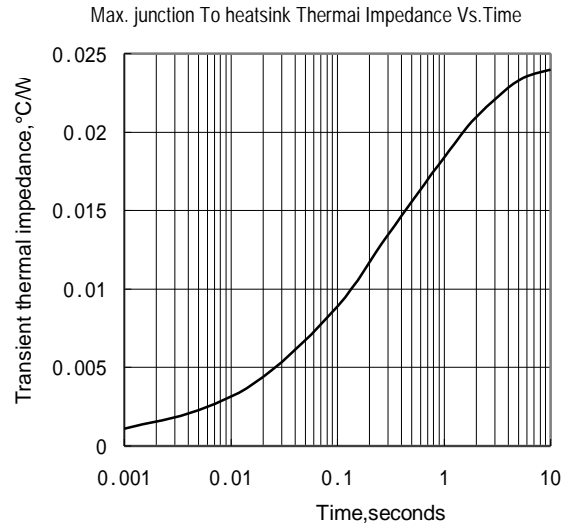


Fig.2

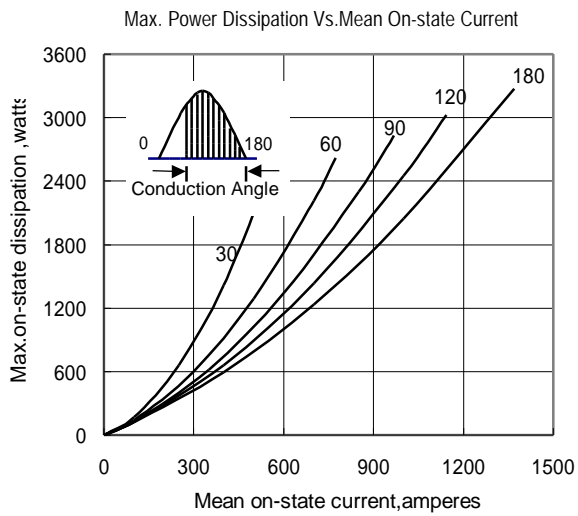


Fig.3

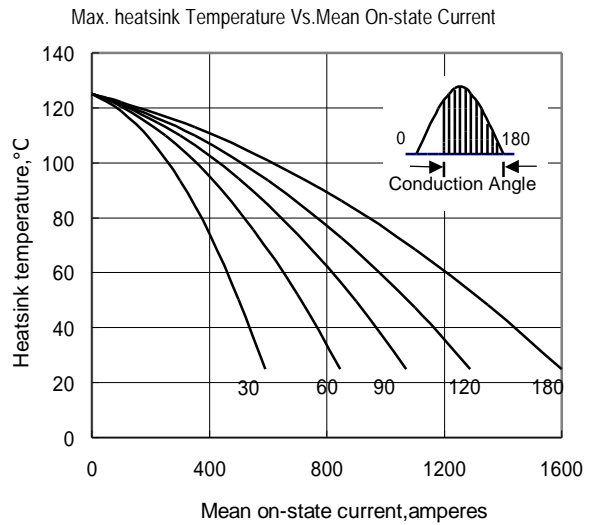


Fig.4

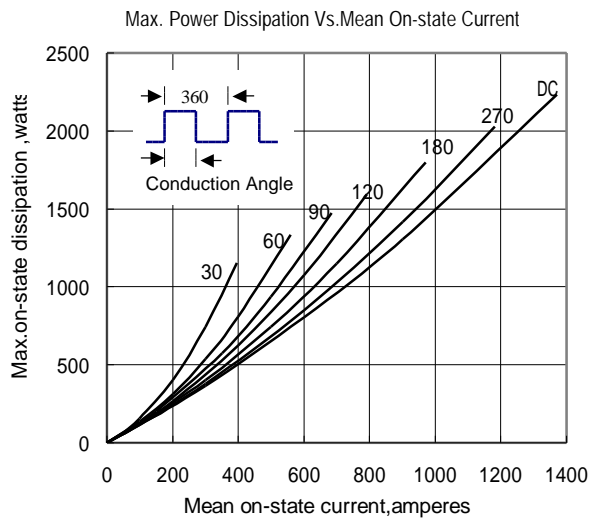


Fig.5

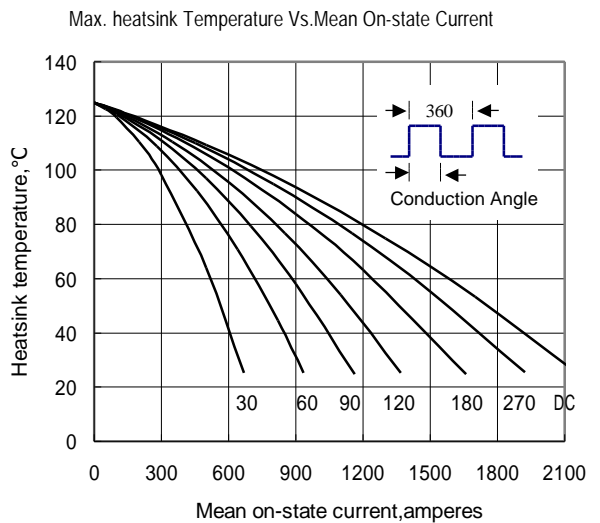


Fig.6

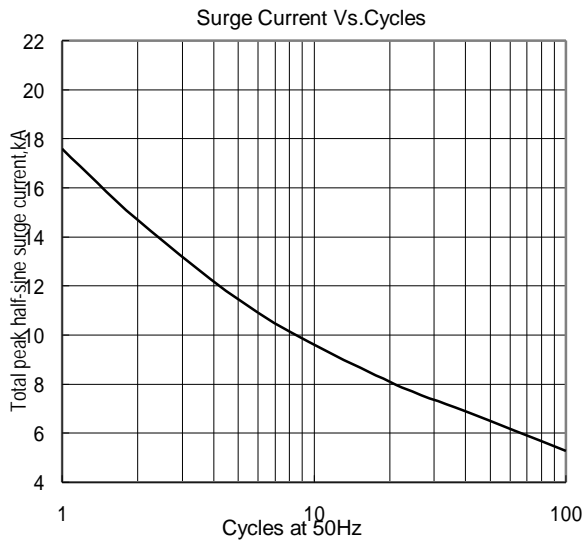


Fig.7

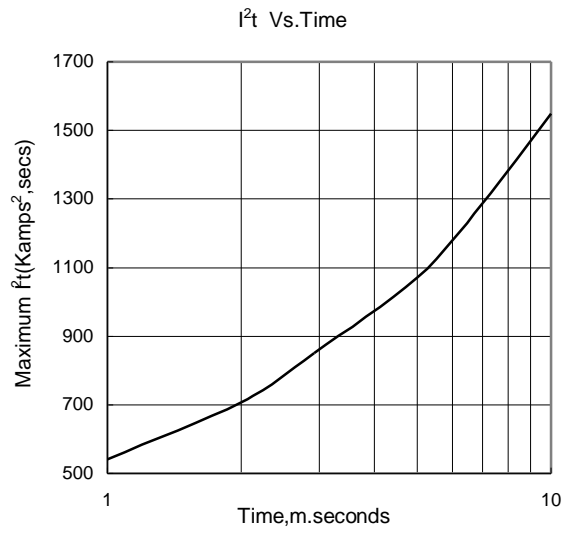


Fig.8

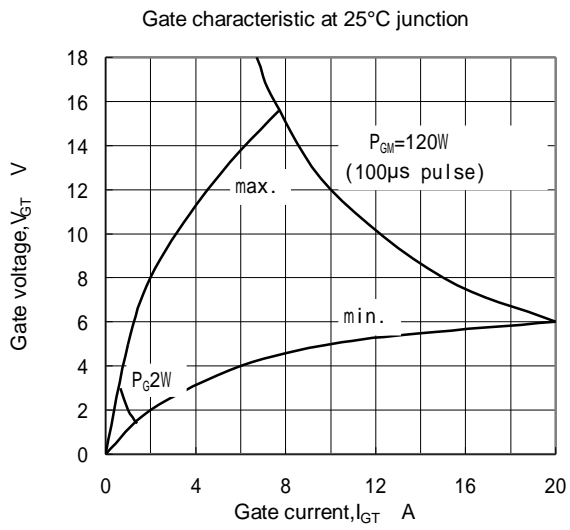


Fig.9

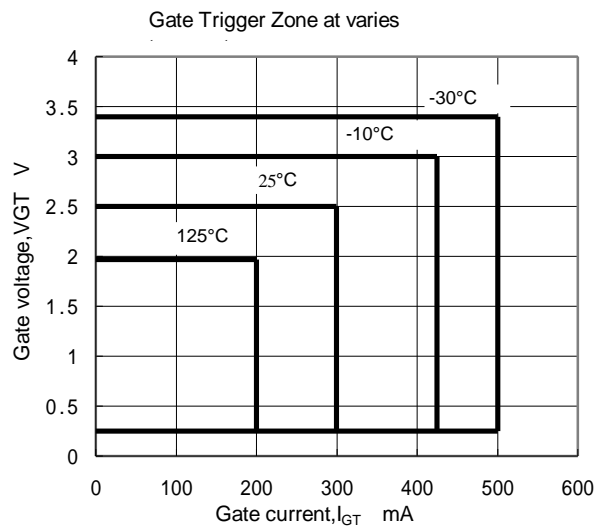


Fig.10