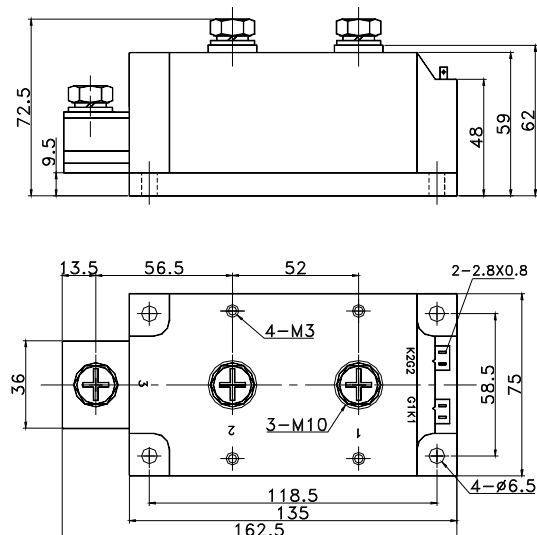
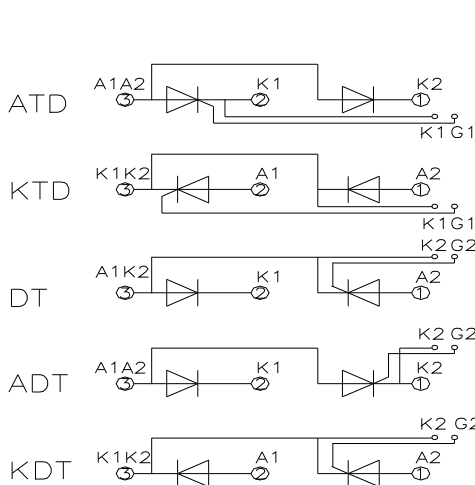


TD400 ATD400 KTD400 DT400 ADT400 KDT400

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T <sub>j</sub> (°C)	VALUE			UNIT
				Min	Type	Max	
I <sub>T(AV)</sub> I <sub>F(AV)</sub>	Mean on-state current	180° half sine wave 50Hz Single side cooled, T <sub>C</sub> =85°C	125			400	A
I <sub>T(RMS)</sub>	RMS on-state current	Single side cooled, T <sub>C</sub> =85°C	125			628	A
V <sub>DRM</sub> V <sub>RRM</sub>	Repetitive peak off-state voltage Repetitive peak reverse voltage	V <sub>DRM</sub> &V <sub>RRM</sub> tp=10ms V <sub>DSM</sub> &V <sub>RSM</sub> = V <sub>DRM</sub> &V <sub>RRM</sub> +200V respectively	125	600		1800	V
I <sub>DRM</sub> I <sub>RRM</sub>	Repetitive peak current	at V <sub>DRM</sub> at V <sub>RRM</sub>	125			40	mA
I <sub>TSM</sub>	Surge on-state current	10ms half sine wave	125			12.0	KA
I <sup>2</sup> t	I <sup>2</sup> T for fusing coordination	V <sub>R</sub> =60%V <sub>RRM</sub>				734	A <sup>2</sup> s*10 <sup>3</sup>
V <sub>TO</sub>	Threshold voltage		125			0.80	V
r <sub>T</sub>	On-state slop resistance					0.49	mΩ
V <sub>TM</sub>	Peak on-state voltage	I <sub>TM</sub> =1200A	125			1.52	V
dv/dt	Critical rate of rise of off-state voltage	V <sub>DM</sub> =67%V <sub>DRM</sub>	125			800	V/μs
di/dt	Critical rate of rise of on-state current	From 67%V <sub>DRM</sub> to 1200A, Gate source 1.5A t <sub>r</sub> ≤0.5μs Repetitive	125			100	A/μs
I <sub>GT</sub>	Gate trigger current			30		200	mA
V <sub>GT</sub>	Gate trigger voltage	V <sub>A</sub> =12V, I <sub>A</sub> =1A	25	1.0		3.0	V
I <sub>H</sub>	Holding current			20		100	mA
V <sub>GD</sub>	Non-trigger gate voltage	At 67%V <sub>DRM</sub>	125			0.2	V
R <sub>th(j-c)</sub>	Thermal resistance Junction to heatsink	At 180° sine' Single side cooled				0.080	°C /W
V <sub>iso</sub>	Isolation voltage	50Hz, R.M.S, t=1min, I <sub>iso</sub> :1mA(MAX)		2500			V
F <sub>m</sub>	Thermal connection torque(M10)					0.60	N·m
	Mounting torque(M6)					0.30	N·m
T <sub>stg</sub>	Stored temperature			-40		140	°C
W <sub>t</sub>	Weight					2300	g
Outline	408F3						

OUTLINE DRAWING & CIRCUIT DIAGRAM



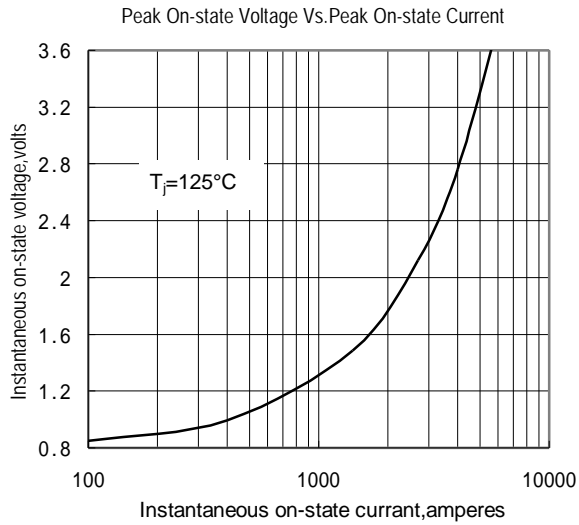


Fig.1

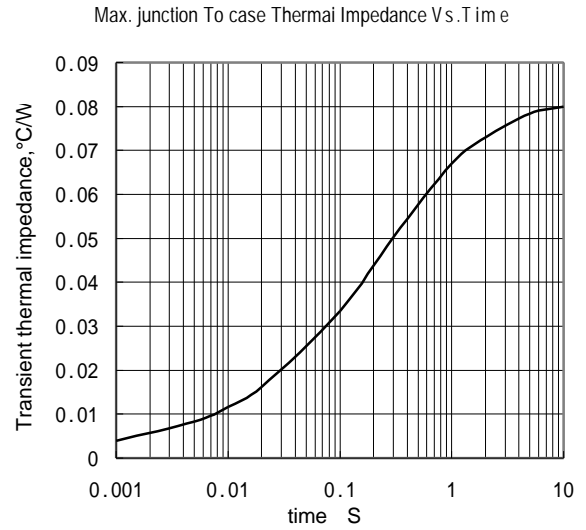


Fig.2

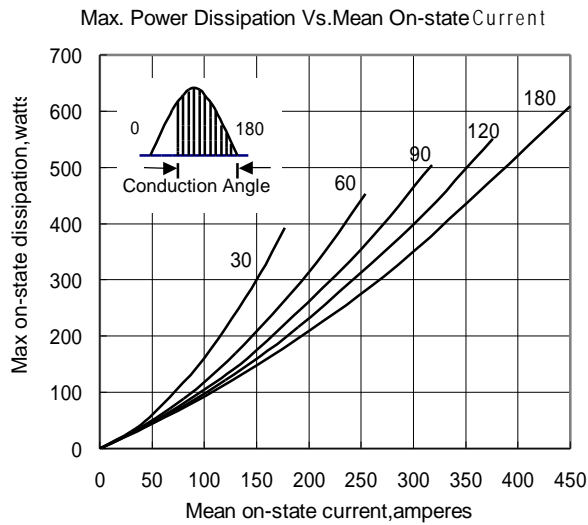


Fig.3

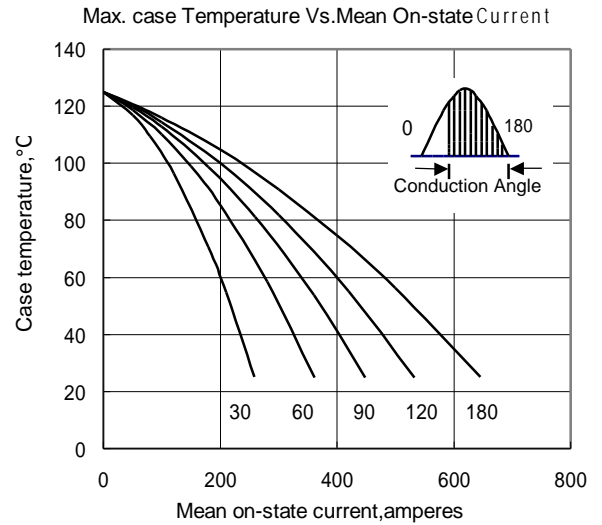


Fig.4

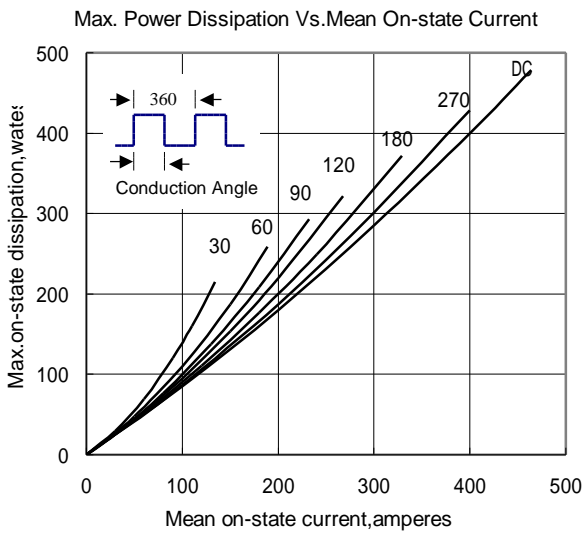


Fig.5

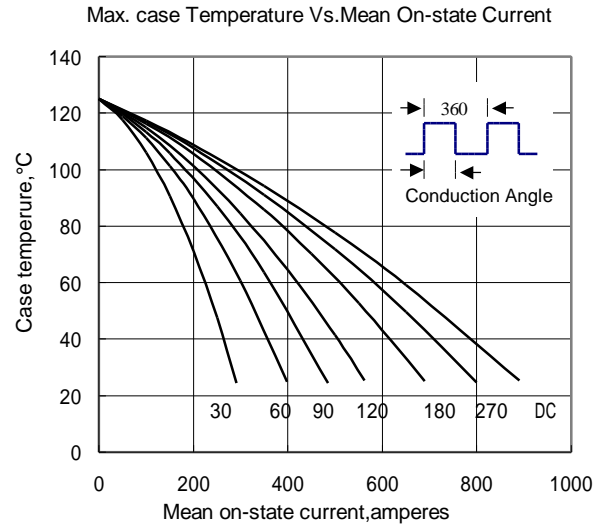


Fig.6

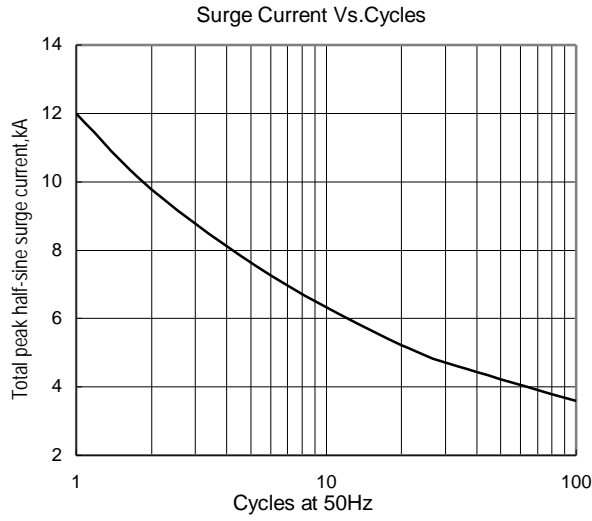


Fig.7

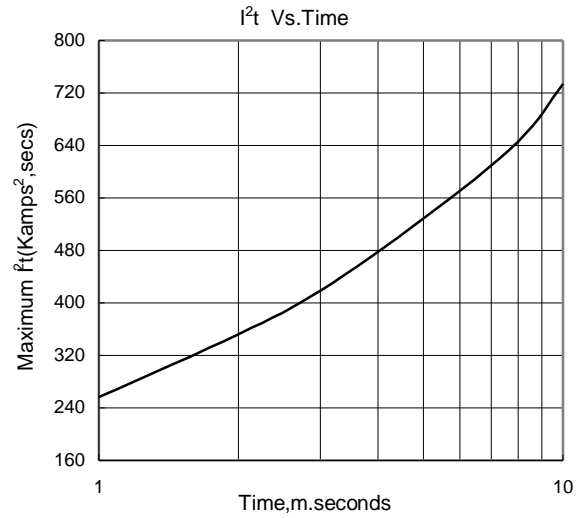


Fig.8

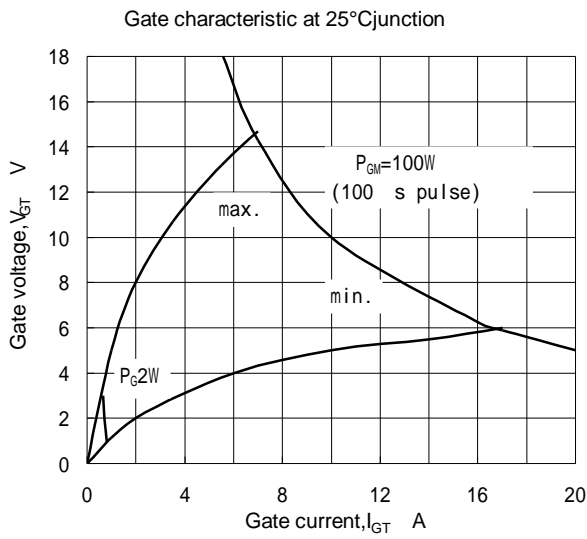


Fig.9

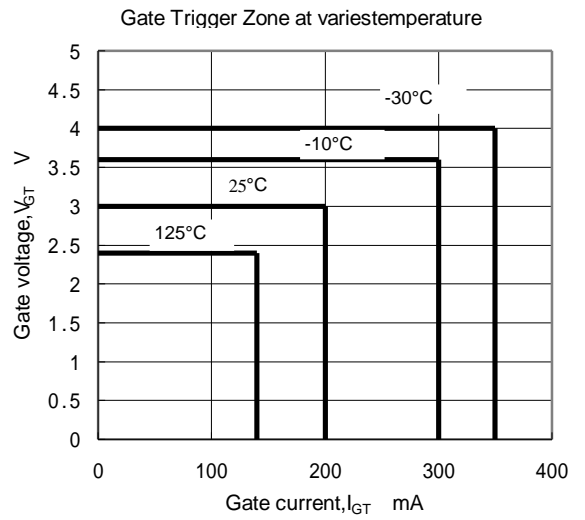


Fig.10